SEMARAK ILMU
PUBLISHING
202103268166(003316878-P)

Journal of Advanced Research in Applied Sciences and Engineering Technology

Journal homepage:
https://semarakilmu.com.my/journals/index.php/applied_sciences_eng_tech/index
ISSN: 2462-1943

CMOS Based ESD Protection Circuit for Low Voltage

Awang Azfanurisham Awang Zaidil[1,*], Warsuzarina Mat Jubadi[2], Nabihah@Nornabilah Ahmad[2]

[1] Department of SMD Microelectronic Sdn. Bhd., Kota Samarahan, Sarawak, Malaysia
[2] Department of Electronic Engineering, Faculty of Electrical and Electronic Engineering, University Tun Hussien Onn Malaysia, Batu Pahat, Malaysia

ARTICLE INFO

Article history:
Received 27 November 2026
Received in revised form 20 February 2026
Accepted 15 April 2026
Available online 4 May 2026

Keywords:
Electrostatic Discharge (ESD); Protection circuit; Human Body Model (HBM) test; Complementary Metal Oxide Semiconductor (CMOS); Cadence Electronic Design Automation (EDA)

ABSTRACT

Electrostatic discharge (ESD) is a common phenomenon, poses a risk to devices and circuits due to their high energy transfer. Catastrophic or latent failures in ICs can result from ESD damage, with latent damage potentially causing malfunctions or premature failure. To safeguard against ESD, protection methods and schemes, such as CMOS - based approaches, are implemented to divert and minimize high currents and voltages, especially as IC technology advances to smaller scales. This project proposed a protection scheme based on 45 nm CMOS technology which was done in Cadence EDA tools. CMOS structures and clamping diode with the implementation of inverter were utilized to reduce peak discharge current and mitigate ESD damage through fast rise times. The Human Body Model (HBM) which is equivalent to 2 kV was used as a testbench for the protection circuit. The first peak current (31.169 mA) of proposed design has results in 97.66 % reduction with the rise time of 55.58 fs, fall time 2.188 ps, and a peak discharge current period of 174.66 fs. The total power dissipation for the DUT is 29.15 mW with circuit layout of 16.81 nm^2. In summary, the proposed ESD protection circuit can be implemented in the low voltage application.

1. Introduction

Electrostatic discharge (ESD) is a phenomenon characterized by the rapid transfer of charges between objects, leading to high voltage and current levels that can cause significant damage to devices and circuits [1-2]. To prevent ESD damage, one approach is to divert the ESD current away from the main circuits, input/output (I/O) ports, and power sources by adding a low impedance clamp circuit [3]. ESD-induced current can cause various issues such as thin film burnout, junction filamentation, and junction spiking, leading to permanent malfunctioning of devices [4]. Charge injection and breaking of the oxide layer can also occur due to ESD-induced voltage, resulting in latent damage that may not immediately affect device performance [4]. As technology nodes for ICs become smaller, the susceptibility of complementary metal-oxide semiconductor (CMOS) devices to

---

[*] *Corresponding author.*
E-mail address: Awangaz@smdsemiconductor.com

https://doi.org/10.37934/araset.59.5.139151

ESD failure increases due to thinner gate oxides and shallower junctions [5-7]. To design effective ESD protection, ESD events can be simulated using models such as the Human Body Model (HBM), Machine Model (MM), and Charged Device Model (CDM) [8]. These models mimic real-world ESD events and help in the design process. Several approaches can be employed to protect circuits from ESD, including the design of ESD protection circuits, utilization of ESD protection devices, adherence to ESD control and handling protocols, and the use of ESD protection integrated circuits (ICs) [9-10]. Designing circuits with materials and structures resistant to ESD, such as Silicon-On-Insulator (SOI) technology, can enhance ESD protection [10]. ESD protection devices like diodes or transistors can be integrated into the circuit to safely dissipate ESD current and prevent damage [10]. The discharging clamp circuit is also known as the power clamp due to the design allowing the discharging path between the power line VDD and VSS which will optimize the overall discharging process when an ESD event occurs [11]. One of the most popular power clamps is the three-stage RC delay. Three inverters are connected in series with an RC detecting component to create the delay buffer as shown in Fig.1.

Diode is the most common device for ESD protection circuit due to its high protection efficiency when it is in forward bias. Aside from that, Zener diodes could also be used as a protection device when implementing it in reverse bias mode [13-14]. Due to the low turn on voltage characteristics, diodes are usually stacked in order to withstand a higher voltage node [11]. The I-V characteristics of a diode are shown in Fig. 2. One downside of diodes is that they have a large leakage current as compared to the other ESD protection devices which will then increase its power consumption.

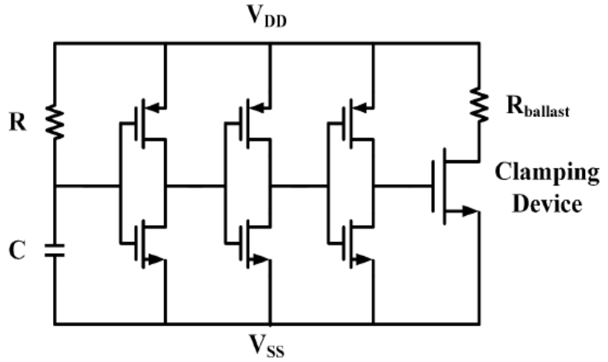


Fig.1. Equivalent power clamp protection scheme using three stage RC delay [12]

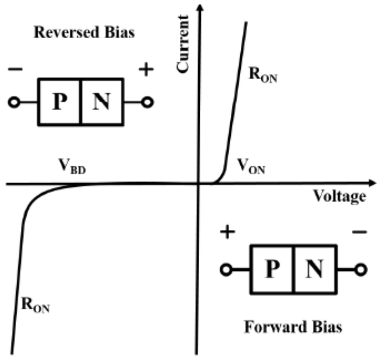


Fig. 2. Current-Voltage characteristics for diode [11]

CMOS technology consists of two most significant IC devices, PMOS and NMOS, as they are also helpful in the ESD protection design. P-type and n-type transistors are both employed in CMOS circuits as shown in Fig.3. A p-type semiconductor is a substance that lacks electrons and is used to make p-type transistors. The n-type transistors, on the other hand, are constructed from a substance known as an n-type semiconductor that has an overabundance of electrons [11]. The equivalent circuit for the HBM ESD is shown in Fig. 4.

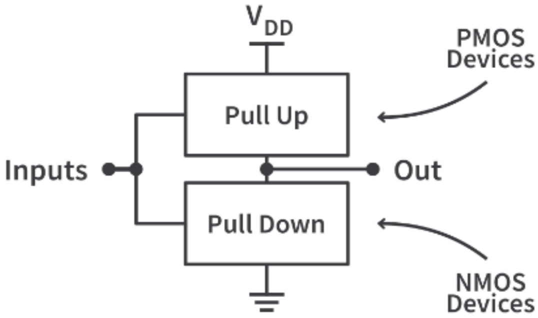


Fig. 3. I-V characteristics for diode

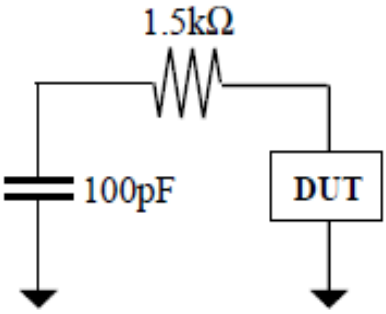


Fig. 4. Simplified HBM equivalent circuit [4]

In the human body, there are initially static charges that are being stored and could be transferred into an Integrated Circuit just by touching the ICs. The standard for any ESD protection circuit is that it could sustain at least 2 kV HBM ESD stress which could generate an ESD peak current of around 1.3 A and a rise time of around 10 ns with a decay time of 130 ns to 170 ns [15]. There are a few important parameters in the HMB equivalent circuit which include an ESD capacitor of 100 pF and an ESD resistor of 1500 Ω [4].

Table 1 shows the classification of HBM standards published by JEDEC which were according to the threshold voltage in the HBM testing [11].

Table 1
HBM classification based on JEDEC.

Classification	Voltage range (V)
0	< 250
1A	250 to < 500
1B	500 to < 1000
1C	1000 to < 2000
2	2000 to < 4000
3A	4000 to < 8000
3B	> 8000

Various studies have proposed ESD protection circuit designs using different CMOS processes and structures. For example, a 40 nm CMOS process was used to design an ESD clamp circuit for input transistors, which demonstrated improved ESD robustness with current withstand capacities of 2 A (NMOS) and 1.4 A (CMOS) [16]. Another study [17] investigated optimal ESD structures using a 0.35 µm CMOS technology and showed significant reductions in peak current through the implementation of protective circuits. A 28 V ESD clamp circuit occupying 0.21 mm^2 was designed using a 40 nm CMOS process and achieved a maximum leakage current of 3 mA, withstanding 6 kV HBM testing [18]. Latch-up-free ESD protection designs using SCR and CMOS were presented, demonstrating fast turn-on times and high ESD levels in a 130 nm CMOS process [19]. Resistor-less power-rail ESD clamp circuits with ultra-low leakage current and standby leakage current were proposed and verified in a 65 nm CMOS process [20-21]. Overall, these studies highlight the development of ESD protection circuits using various CMOS processes and structures to enhance ESD robustness and prevent damage in ICs. Different widths of SCR and CMOS structures have been explored, achieving significant improvements in ESD performance and current withstand capacities.

2. Methodology

2.1 Proposed CMOS-Based ESD Protection Circuit Architecture

Fig.5 illustrates the block diagram for the CMOS-based ESD protection circuit which consists of diodes as clamping devices and CMOS. Meanwhile, Fig. 6 shows the proposed design schematic for the ESD protection circuit which consists of diodes, PMOS, NMOS, and resistors. In this design, it implements the CMOS ESD protection device with an additional clamping diode. The additional diodes shunt the transient current to VCC and Ground power supply line which reduces the excessive voltage that could damage the internal circuit.

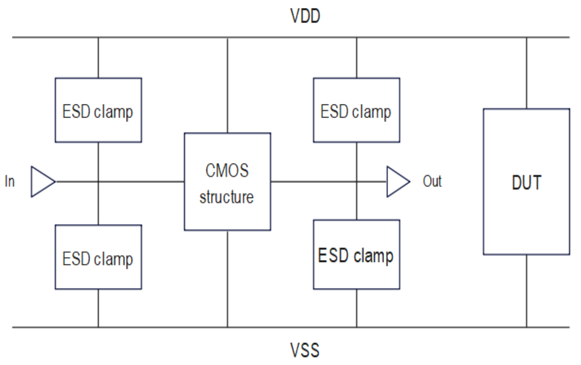


Fig. 5. Block diagram of CMOS-based ESD protection structure

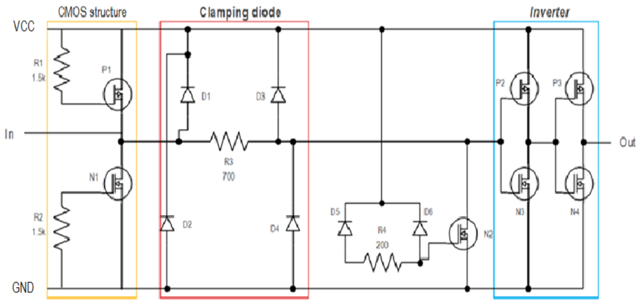


Fig. 6. CMOS based ESD protection circuit.

The resistors that are placed in between the clamping diodes will limit the peak current. The resistors are carefully selected with regards to the fact that the usage of large series resistance and large junction capacitance of ESD clamp devices results in a prolonged resistance-capacitance (RC) delay for input signals, which is not desirable for high-precision circuit applications.

Besides, the complexity of the design process increased as well, necessitating accurate CMOS circuit modelling. The gate length and gate oxide of MOS transistors have been two critical aspects in improving the vulnerability of CMOS devices. The proposed protection structure includes the clamping diode and gate coupling which limits the voltage and current while at the same time diverting the ESD current. Besides, the gate coupling method is used to reduce the overstress voltage and protect the thin gate oxide. The size of N1 and P1 transistors must be designed with large dimensions so that it can withstand the high ESD level which in this case, P1: 100 µm (W) /150 nm (L) and N1: 50 nm (W) /150 nm (L). The width size of the transistors for PMOS must be doubled from the NMOS since the rise time and fall time of the gate should be equal. Furthermore, resistors R1 and R2 need to limit the ESD current flowing through the short channel of the transistor efficiently. Besides, due to the high-precision issues, the value for the resistance should not be large, thus the value R1 and R2 were chosen as 750 Ω while R3 and R4 values are 350 Ω and 100 Ω, respectively. Table 2 illustrates the parameters for the overall device that are implemented in the ESD protection circuit.

Table 2
Device parameter FOR ESD protection circuit

Device / Component	Values
R1	750 Ω (W = 1 µm / L = 50 µm)
R2	750 Ω (W = 1 µm / L = 50 µm)
R3	350 Ω (W = 1 µm / L = 23.335 µm)
R4	100 Ω (W = 1 µm / L = 6.67 µm)
P1	W = 100 µm / L = 150 nm
P2	W = 800 nm / L = 150 nm
P3	W = 800 nm / L = 150 nm
N1	W = 50 µm / L = 150 nm
N2	W = 400 nm / L = 150 nm
N3	W = 400 nm / L = 150 nm
N4	W = 400 nm / L = 150 nm

CMOS based ESD protection circuit is encapsulated into the HBM equivalent circuit as shown in Fig.7. The HBM analysis is intended to investigate the reliability and robustness of the protection structure using CMOS technology in an ESD events.

In the HBM test circuit, it imitates the ESD phenomenon from human body that is electrostatically charged contacted a chip and then form a discharge path. Two important parts in this implementation are the resistor and capacitor which are equivalent with the resistance value of 1.5 kΩ while the capacitance of 100 pF indicates the static charge carried by a human body while the V_{pulse} is varied depending on the test which in this case 2 kV is chosen.

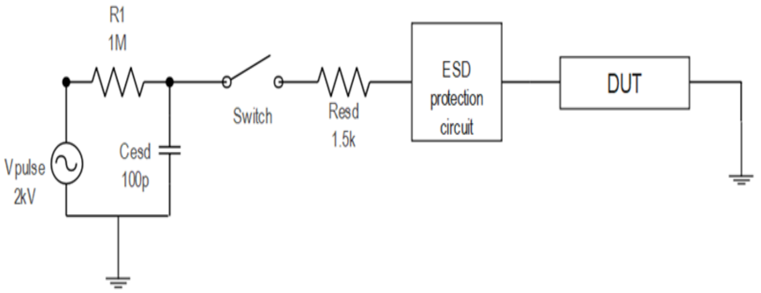


Fig. 7. Equivalent HBM testing of the CMOS based ESD protection circuit

The resistor R1 is used to reduce the incoming voltage from source which is one of the reasons that the value for this resistor is low. Table 3 lists the components parameters for the purpose of testing using HBM model.

Table 3
Components parameter for the HBM test circuit

Component	Values
Pulse Voltage	2 kV

Resistor 1	1 MΩ
ESD resistor	1.5 kΩ
ESD capacitor	100 pF
DUT resistor	30 Ω

2.1 Power dissipation to the Device Under Test (DUT)

Power dissipation refers to the amount of electrical power that is absorbed by the DUT during an ESD event. When an ESD event occurs the high voltage discharge could cause rapid current flow through the DUT which will eventually cause localized heating and high risk of malfunction to the DUT. The power dissipation to the device under test can be expressed by using (1), where the $i^2(t)$ is the discharge current value and RDUT is the resistance value for the device under test.

$$P(t) = i^2(t) \times \mathrm{RDUT} \tag{1}$$

3. Results

The Human Body Model is used to simulate ESD protection circuits, which turns out to be an important task. This section delves into the findings from HBM simulations, illuminating how the addition of ESD protection circuits affects the behaviour of devices exposed to ESD events brought on by human touch. The durability of the device can be ensured by incorporating these circuits, which can limit any potential ESD damage.

3.1 Simulation of ESD protection circuit using HBM model

The analysis of HBM simulation using ESD protection circuits is an important aspect of designing a robust and reliable electronic device. HBM simulation allow engineers to understand and evaluate the behaviour of devices when subjected to ESD events caused by human touch. By incorporating ESD protection circuits into the design which could mitigate the potential damage caused by ESD and ensure the longevity of the device.

This transient analysis involves studying the response of the circuit during HBM simulation, including the current and voltage levels experienced by the device. By simulating the HBM scenario, the effectiveness of the ESD protection circuits in diverting the ESD current away from critical components and preventing damage can be measured and analysed. Fig. 8 shows the schematic of the CMOS-based ESD protection circuit which is done in the Cadence EDA tools and has been verified its electrical rule.

Fig. 9 illustrates the implementation of the protection circuit in the HBM model for the purpose of testing. The test was conducted in Cadence Virtuoso ADE L by using 2kV voltage pulse to simulate the charge human body. Besides, 3.3V power supply is used to power the protection circuit. The discharge current that represents the peak current for 2 kV voltage which are equivalent to 1.33 A is applied on the input of the protection circuit.

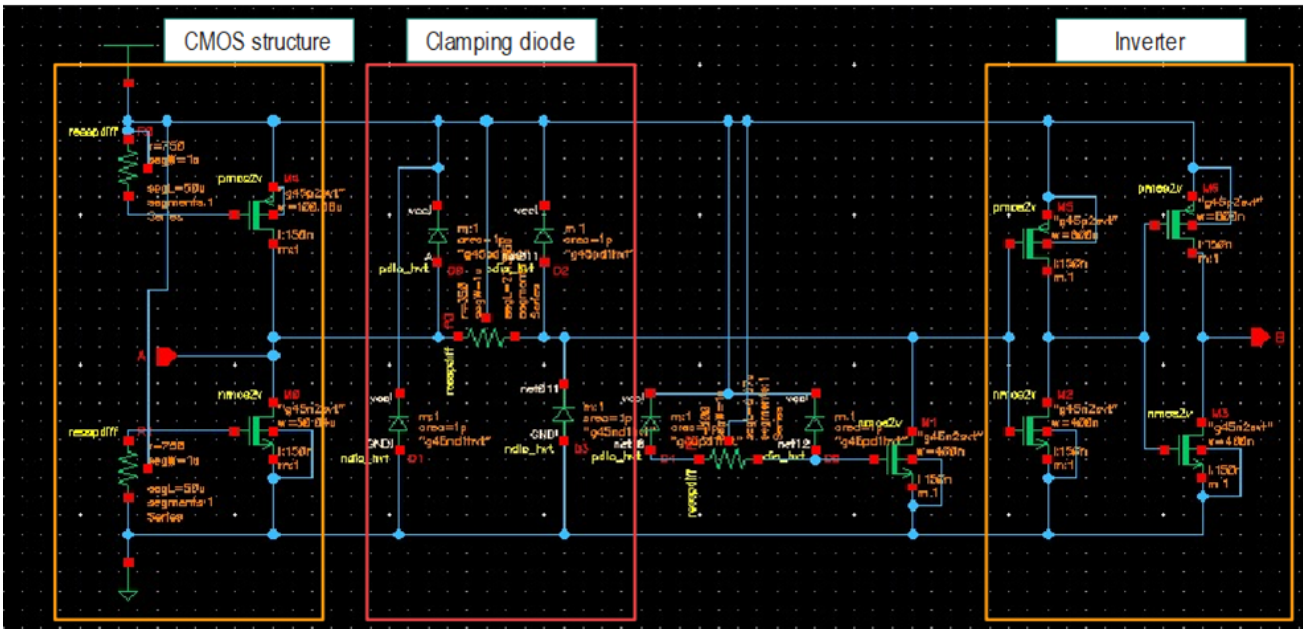


Fig. 8. Schematic of the CMOS based ESD protection circuit implemented in Cadence EDA tools

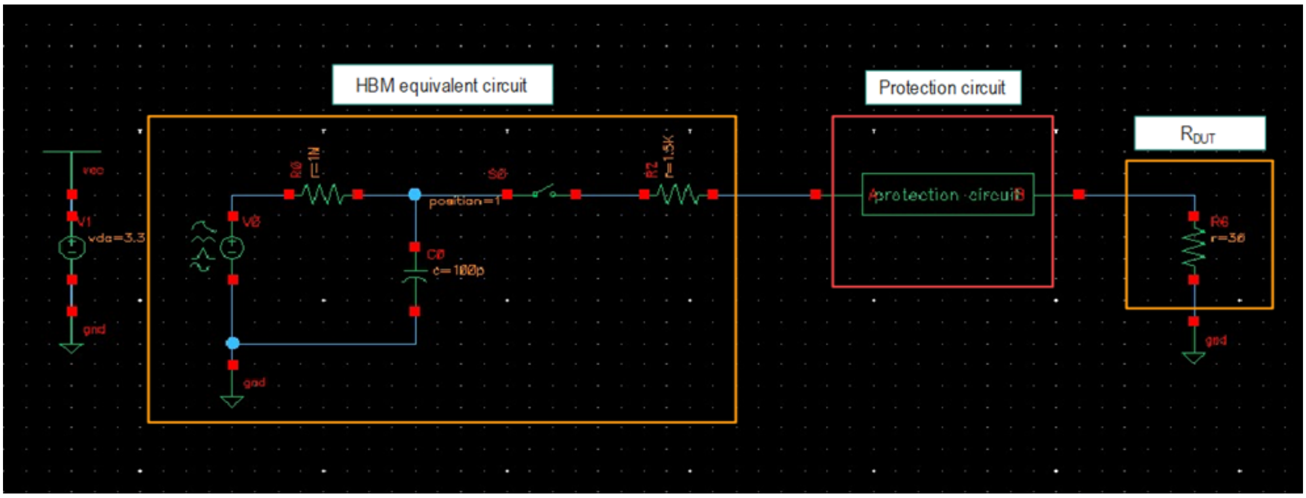


Fig. 9. Protection circuit implementation in the HBM model using Cadence EDA tools

3.2 Transient response of ESD protection circuit

Based on the simulation waveform that was obtained in the implementation of the protection circuit has resulted in a significant reduction in the peak discharge current as shown in Fig. 10. Prior to the implementation of the protection circuit, the peak current was measured at 1.33 A, indicating the maximum amount of current flowing through the circuit during its operation. However, after the protection circuit was introduced, the peak current decreased to 31.169 mA, which is equivalent to 97.66 % representing a substantial decrease in the magnitude of the current.

Fig. 11 show an the discharge current waveform with the rise time and fall time after the protection circuit was introduced. Rise time and fall time before the protection circuit are 17.44 fs and 185.5 ns respectively while after the implementation of the protection circuit, the rise time is 55.58 fs and fall time 2.188 ps.

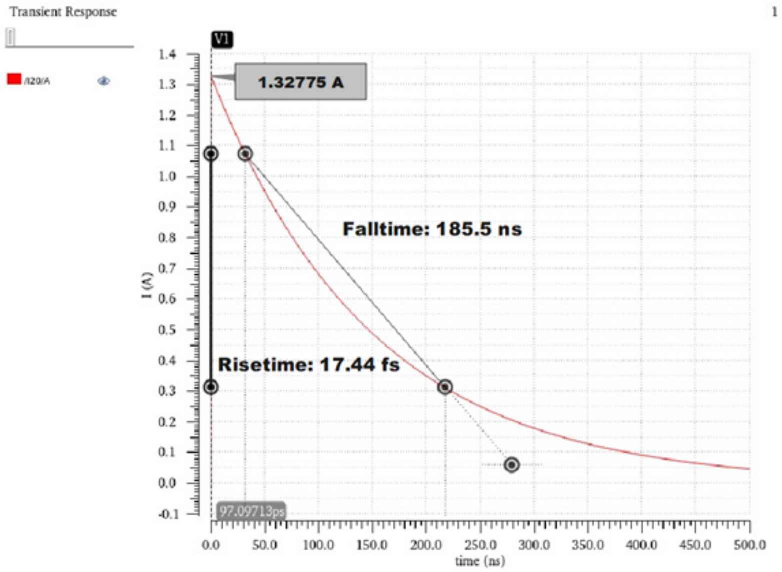


Fig. 10. Discharge current waveforms of peak current with rise time and fall time of conventional HBM waveform (without protection circuits)

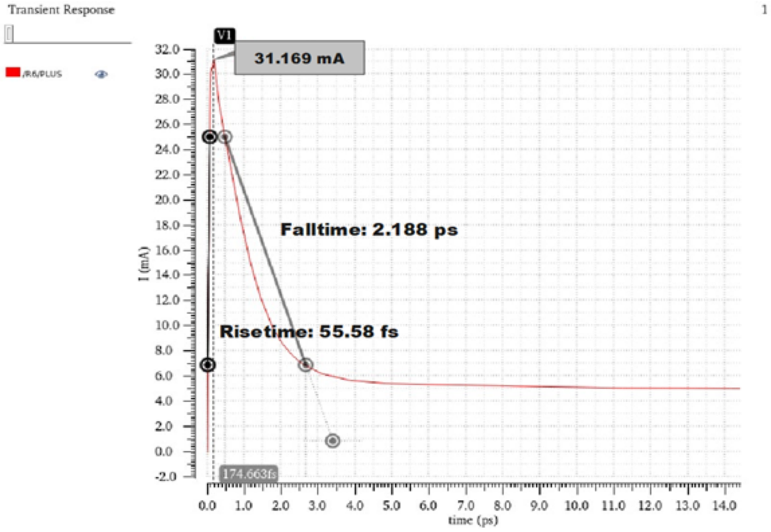


Fig. 11. The overall waveform of peak current with rise time and fall time of the HBM test using the proposed protection circuits.

The peak discharge current represents the maximum amount of current flowing through the circuit as presented in Fig.10 and Fig. 11 was significantly reduced from 1.33 A to 31.169 mA which equivalent to 97.66 % decrease of current. In the previous work [17], the peak current was measured at 1.25 A (without protection circuit) while it decreases to 56.8 mA which equivalent to 95.46 % reduction with circuit protection. Hence, the proposed protection circuit\ effectively limits the current to a safer level, preventing potential damage to the circuit.

Similarly, the peak discharge current period, which measures the time taken for the current to reach maximum value before declining. Prior to the implementation of protection circuit, the peak discharge current period was measured at 97.1 ps. This value significantly reduced to 174.7 fs (with protection circuit), indicating faster time to reach maximum current. Furthermore, the peak discharge current period increased from 12.8 ns to 47.5 ns [17]. These results indicate that the proposed design achieves a greater reduction in time taken to reach maximum discharge current.

In addition, the rise time was measured at 17.44 fs (without protection circuit), indicating the time it takes for the signal to transition from the low level to the high level. However, the rise time slightly increased to 55.58 fs with protection circuit implementation. Similarly, the fall time, which measures the signal's transition from the high level to the low level, also experienced a noticeable change. Initially, the fall time was measured at 185.5 ns. However, after the protection circuit was incorporated, the fall time significantly decreased to 2.188 ps, indicating a much faster signal transition. These changes in rise and fall times highlight the effectiveness of the protection circuit in optimizing the signal performance. The circuit has successfully enhanced the speed at which the signal rises and falls, thereby improving the overall reliability of the system.

By obtaining the discharge current value from the simulation, we can calculate the power dissipation to the DUT using (1). Based on the proposed protection circuit peak discharge current value, the power dissipation is measured at 29.15 mW which is smaller than the conventional HBM testing without any protection circuit that is 53.07 W. RDUT value of 30 Ω in [17] is assumed equal to the one that are used in the proposed design, the power dissipation obtained for the DUT is 96.79 mW.

Table 3 presents the comparison between the proposed ESD protection circuit with the previous work [17]. Based on the proposed design, the power obtained is 29.15 mW while higher power (96.79 mW) was gained in [17].

Table 4
Proposed ESD protection circuit comparison to the previous work in [17]

	Proposed design	**Previous work [17]**
Technology node (nm)	45	350
HBM testing (kV)	2	2
Peak current (mA)	31.169	56.8
Current reduction (%)	97.66	95.46
Rise time (s)	55.58 f	-
Fall time (s)	2.188 p	-
Peak discharge current period (s)	174.66 f	47.5 n
Power dissipation (mW)	29.15	96.79

3.3 Layout of ESD protection circuit

Fig. 12 illustrates the layout of the proposed ESD protection circuit. The layout is then needed to undergo the physical verification steps such as DRC, LVS, ERC, and PEX to make sure it is free from any error. Furthermore, if the layout is not debugged properly, the layout will not work as schematic design. The overall size of the layout is 16.81 nm^2, where the width is 130.55 µm and the length is 128.78 µm.

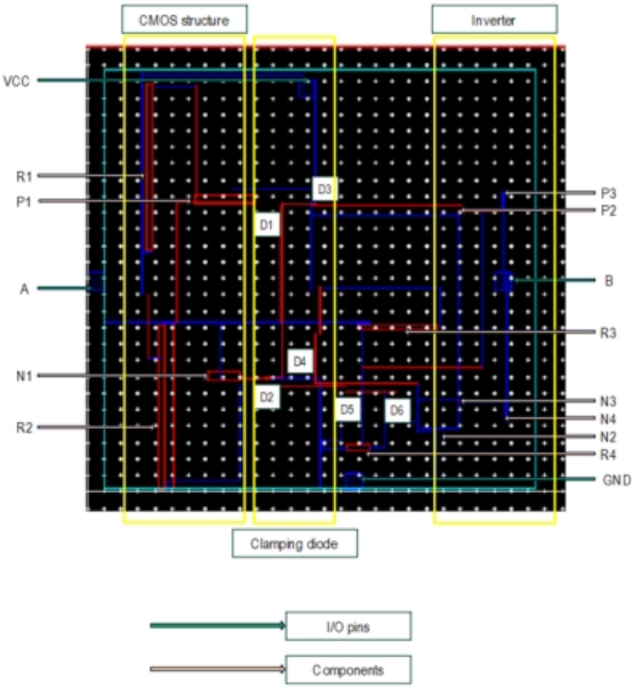


Fig. 12. Layout of the proposed ESD protection circuit

The MOSFETS layout of PMOS and NMOS (P2, P3, N2, N3, and N4) were chosen from the Cadence gpdk045 library which in this case the pmos2v and nmos2v are used. The PMOS and NMOS will have 3 terminals consisting of Gate, Drain and Source with one extra connection which is bulk that are connected on either the VCC or ground depending on the connection. The bulk needs to be connected to the correct terminals to avoid any error in DRC stage. Some of the common errors for PMOS and NMOS are the latch-up error and p-well stamp error connect.

3.3 Layout of ESD protection circuit

The results of Design Rule Checker (DRC) using Assura are shown in Fig. 13. The DRC step is passed without any error indicating that the proposed layout has met the requirement which includes the minimum metals width, minimum spacing, minimum enclosure, etc. The results of Layout versus Schematic (LVS) using Assura are shown in Fig. 14. The LVS step is passed without any error and mismatched between schematic and layout. The LVS process is where the comparison between layout and schematic is conducted to make sure that all the components and netlists are identical. Some of the common errors in LVS are the unmatched nets, unmatched pins, and parameters mismatched.

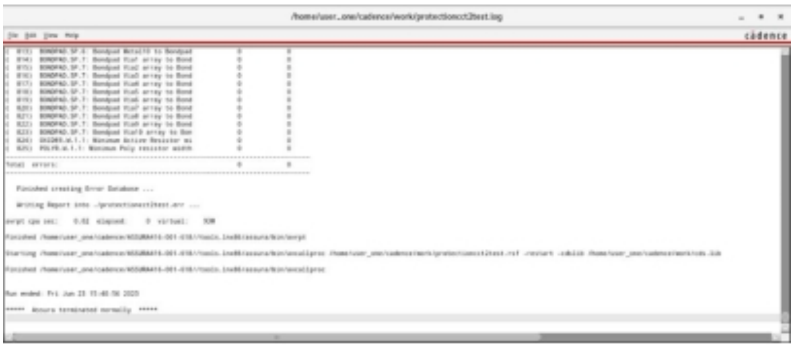
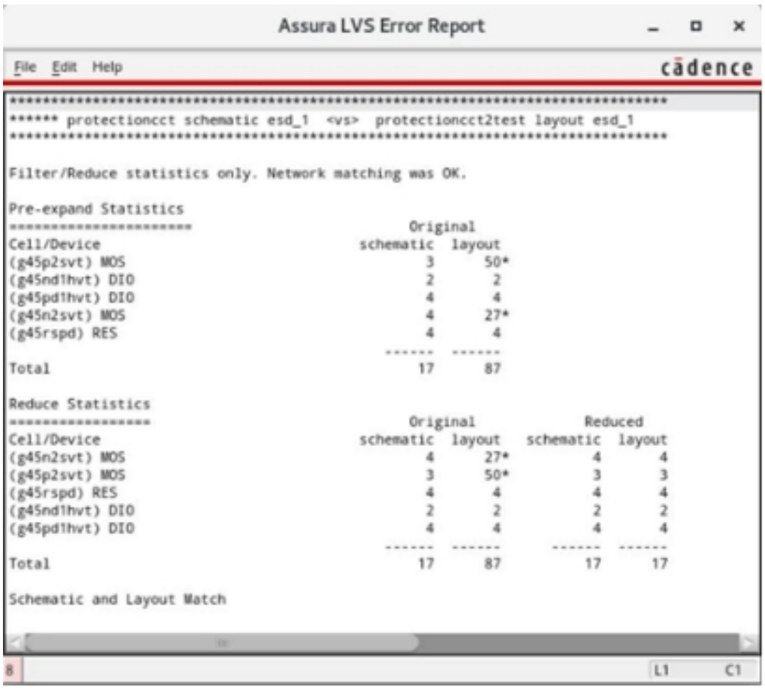


Fig. 13. DRC log result



```
*******************************************************************************
****** protectioncct schematic esd_1  <vs>  protectioncct2test layout esd_1
*******************************************************************************

Filter/Reduce statistics only. Network matching was OK.

Pre-expand Statistics
======================
                                                Original
Cell/Device                               schematic  layout
(g45p2svt) MOS                                    3      50*
(g45nd1hvt) DIO                                   2       2
(g45pd1hvt) DIO                                   4       4
(g45n2svt) MOS                                    4      27*
(g45rspd) RES                                     4       4
                                             ------  ------
Total                                            17      87

Reduce Statistics
=================
                                                Original             Reduced
Cell/Device                               schematic  layout   schematic  layout
(g45n2svt) MOS                                    4      27*          4       4
(g45p2svt) MOS                                    3      50*          3       3
(g45rspd) RES                                     4       4           4       4
(g45nd1hvt) DIO                                   2       2           2       2
(g45pd1hvt) DIO                                   4       4           4       4
                                             ------  ------      ------  ------
Total                                            17      87          17      17

Schematic and Layout Match
```

Fig. 14. LVS log result

4. Conclusions

This project expand the awareness of the ESD damage towards electronics devices under certain circumstances which are gained from the review of previous research, website and resources. The ESD protection circuit can reduce and nullify the high surge of discharge current which will eventually cause damage to the electronic devices in an instance or in a long run. This project consists of two types of design which are the schematic design and layout design. The layout design includes the DRC and LVS part which are successfully drawn in Cadence EDA tools using Asura.

In addition, the overall objectives of this project were achieved which includes the design of a CMOS-based ESD protection circuit that can be implemented in low-voltage electronics applications that are mentioned in the methodology. Next, to verify the functionality of the CMOS structure ESD protection circuit which is stated in the result and discussion. Lastly, to evaluate the performance of CMOS structure ESD protection circuit for low voltage application in terms of the first peak current of discharge and time of discharge current. In conclusion, the proposed CMOS-based ESD protection circuit for low voltage system using 45 nm CMOS technology is constructed and simulated successfully using Cadence EDA tools and the results obtain are in sync with the desired value. The first peak current of the proposed design is 31.169 mA which is equivalent to 97.66 % reduction while implementing the 2 kV voltage pulse with the rise time of 55.58 fs, fall time 2.188 ps, and a peak discharge current period of 174.66 fs. The total power dissipation drawn for the DUT is 29.15 mW with ESD protection circuit layout of 16.81 nm^2.

Acknowledgement

The author would like to thank Universiti Tun Hussein Onn Malaysia for the financial support and Faculty of Electrical and Electronic Engineering, UTHM for the lab facilities access.

References

[1] Vinson, J. E., and J. J. Liou. "Electrostatic discharge in semiconductor devices: Overview of circuit protection techniques." In *Proceedings 2000 IEEE Hong Kong Electron Devices Meeting (Cat. No. 00TH8503)*, pp. 5-8. IEEE, 2000. https://doi.org/10.1109/HKEDM.2000.904204

[2] Wang, Albert, H. Feng, G. Chen, R. Zhan, H. Xie, Q. Wu, and X. Guan. "Key aspects on ESD protection design for ICs: mixed-mode simulation and RF/mixed-signal ESD." In *ASIC, 2003. Proceedings. 5th International Conference on*, vol. 2, pp. 1000-1005. IEEE, 2003. https://doi.org/10.1109/ICASIC.2003.1277380

[3] Semenov, Oleg, Hossein Sarbishaei, and Manoj Sachdev. "ESD devices for input/output protection." *ESD Protection Device and Circuit Design for Advanced CMOS Technologies* (2008): 45-83. https://doi.org/10.1007/978-1-4020-8301-3_3

[4] Oh, Kwang-Hoon. *Investigation of ESD performance in advanced CMOS technology*. Stanford University, 2002.

[5] Wang, Albert ZH. *On-chip ESD protection for integrated circuits: an IC design perspective*. Vol. 663. Springer Science & Business Media, 2002. https://doi.org/10.1007/b117005

[6] Wang, Albert ZH, Haigang Feng, Rouying Zhan, Haolu Xie, Guang Chen, Qiong Wu, Xiaokang Guan, Zhihua Wang, and Chun Zhang. "A review on RF ESD protection design." *IEEE Transactions on Electron Devices* 52, no. 7 (2005): 1304-1311. https://doi.org/10.1109/TED.2005.850652

[7] Liu, Jian, Xin Wang, Hui Zhao, Qiang Fang, Albert Wang, Lin Lin, He Tang et al. "Design and analysis of low-voltage low-parasitic ESD protection for RF ICs in CMOS." *IEEE journal of solid-state circuits* 46, no. 5 (2011): 1100-1110. https://doi.org/10.1109/JSSC.2011.2118290

[8] Semenov, Oleg, Hossein Sarbishaei, and Manoj Sachdev. "ESD Models and Test Methods." *ESD Protection Device and Circuit Design for Advanced CMOS Technologies* (2008): 21-43. https://doi.org/10.1007/978-1-4020-8301-3_2

[9] Voldman, S., D. Hui, L. Warriner, D. Young, R. Williams, J. Howard, V. Gross et al. "Electrostatic discharge protection in silicon-on-insulator technology." In *1999 IEEE International SOI Conference. Proceedings (Cat. No. 99CH36345)*, pp. 68-71. IEEE, 1999. https://doi.org/10.1109/SOI.1999.819858

[10] Luh, Louis, J. Choma, and Jeffrey Draper. "A Zener-diode-activated ESD protection circuit for sub-micron CMOS processes." In *2000 IEEE International Symposium on Circuits and Systems (ISCAS)*, vol. 5, pp. 65-68. IEEE, 2000. https://doi.org/10.1109/ISCAS.2000.857364

[11] Liang, Wei. "Design, Simulation and Characterization of Novel Electrostatic Discharge Protection Devices and Circuits in Advanced Silicon Technologies." (2017).

[12] Semenov, Oleg, Hossein Sarbishaei, and Manoj Sachdev. "ESD Power Clamps." *ESD Protection Device and Circuit Design for Advanced CMOS Technologies* (2008): 117-146. https://doi.org/10.1007/978-1-4020-8301-3_5

[13] Wang, Albert ZH, and Albert ZH Wang. "ESD Protection Device Solutions." *On-Chip ESD Protection for Integrated Circuits: An IC Design Perspective* (2002): 35-71. https://doi.org/10.1007/0-306-47618-5_3

[14] Wang, Albert ZH, and Albert ZH Wang. "ESD Protection Circuit Solutions." *On-Chip ESD Protection for Integrated Circuits: An IC Design Perspective* (2002): 73-106. https://doi.org/10.1007/0-306-47618-5_4

[15] Ker, Ming-Dou, Jeng-Jie Peng, and Hsin-Chin Jiang. "ESD test methods on integrated circuits: an overview." In *ICECS 2001. 8th IEEE International Conference on Electronics, Circuits and Systems (Cat. No. 01EX483)*, vol. 2, pp. 1011-1014. IEEE, 2001. https://doi.org/10.1109/ICECS.2001.957647

[16] Altolaguirre, Federico A., and Ming-Dou Ker. "Active ESD protection for input transistors in a 40-nm CMOS process." In *VLSI Design, Automation and Test (VLSI-DAT)*, pp. 1-4. IEEE, 2015. https://doi.org/10.1109/VLSI-DAT.2015.7114533

[17] Nicuta, Ana-Maria, Oana Costea Beniuga, Paul Dumitru Bicleanu, and Liliana Bargan. "Analysis of ESD protection circuits for high—Performance CMOS structures." In *2012 International Conference and Exposition on Electrical and Power Engineering*, pp. 713-716. IEEE, 2012. https://doi.org/10.1109/ICEPE.2012.6463847

[18] Chowdary, G., F. Neri, S. Somajayula, and G. Notermans. "28V ESD clamp in CMOS 40nm process." In *2012 IEEE International Conference on Electron Devices and Solid State Circuit (EDSSC)*, pp. 1-2. IEEE, 2012. https://doi.org/10.1109/EDSSC.2012.6482885

[19] Wang, Chang-Tzu, Tien-Hao Tang, and Kuan-Cheng Su. "Latch-up free ESD protection design with SCR structure in advanced CMOS technology." In *2011 International Reliability Physics Symposium*, pp. 4C-3. IEEE, 2011. https://doi.org/10.1109/IRPS.2011.5784507

[20] Yeh, Chih-Ting, and Ming-Dou Ker. "Resistor-less power-rail ESD clamp circuit with ultra-low leakage current in 65nm CMOS process." In *2013 IEEE International Reliability Physics Symposium (IRPS)*, pp. EL-2. IEEE, 2013. https://doi.org/10.1109/IRPS.2013.6532071

[21] Wang, Chang-Tzu, and Ming-Dou Ker. "Design of power-rail ESD clamp circuit with ultra-low standby leakage current in nanoscale CMOS technology." *IEEE Journal of Solid-State Circuits* 44, no. 3 (2009): 956-964. https://doi.org/10.1109/JSSC.2008.2012372